Sierra Components, Inc.

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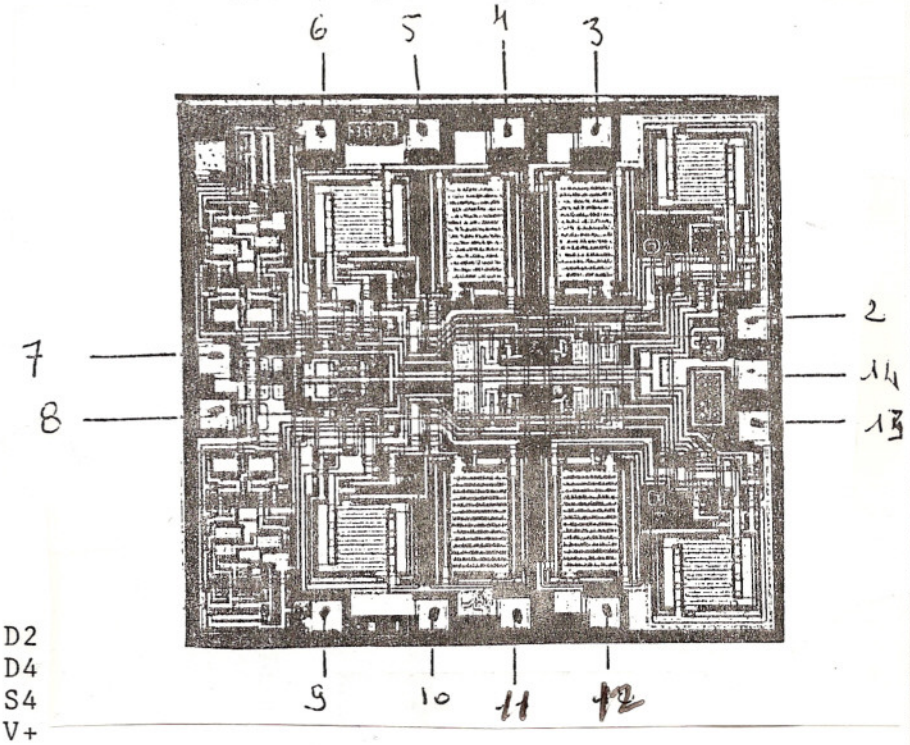
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



DEFINITION :

01-	NC	11-	D2
02-	S3	12-	D4
03-	D3	13-	S4
04-	D1	14-	V+
05-	S1	15-	
06-	IN1	16-	
07-	GND	17-	
08-	V-	18-	
09-	IN2	19-	
10-	S2	20-	

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads : .004" min

APPROVED BY: CD	**DIE SIZE : .081" x .073" +/- 3MILS**	**DATE: 2/5/01**
MFG: Harris	**THICKNESS: .020"**	**P/N: HIO303-2**

DG 10.1.2
Rev A 3-4-99